PATENT

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In re application of: Thomas M. Graettinger Marsela Pontoh Thomas A. Figura	§	
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For: **DOUBLE SIDED CONTAINER CAPACITOR FOR A SEMICONDUCTOR DEVICE AND METHOD FOR FORMING SAME**	§	Atty. Docket: 2003-0236.00/US
	§	Confirmation No.: 7334

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SUBMISSION OF BRIEF ON APPEAL

Please enter this Appeal Brief in response to the Examiner's Final Office Action mailed December 23, 2004 as paper no. 121704 and the Applicants' Notice of Appeal mailed March 23, 2005.

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I. Real Party In Interest

The applicants, Thomas M. Graettinger, Marsela Pontoh, and Thomas A. Figura, have assigned their entire right, title and interest in this application to Micron Technology, Inc. as evidenced by the recordation on July 28, 2003 at reel/frame 014362/0951 of an Assignment to Micron Technology, Inc. by the Applicants.

II. Related Appeals And Interferences

No known related appeals or interferences are pending.

III. Status Of The Claims

Claims 1-28 have been presented during prosecution of the application under appeal;

Claims 13-19 have been canceled as being drawn to a nonelected invention, and;

Claims 1-12 and 20-28 are pending, rejected, and appealed.

IV. Status Of The Amendments

No amendment has been filed by the applicants for the above-captioned case subsequent to the final rejection of September 30, 2005.

V. Summary Of The Claimed Subject Matter

All references in this section are to Applicants' specification and drawings. The statements in this summary are in no way limiting of the scope of the claims, and equivalents.

The present invention addresses a method for forming a semiconductor device capacitor, particularly a double-sided container capacitor, during the formation of a semiconductor device (title and lines 1-2 of ¶[0022]). The embodiment of independent claim 1 comprises providing a base dielectric layer (FIGS. 1 and 8, element 32, and the text at ¶4, line 3 and ¶22, line 4), etching the base dielectric layer to form an opening therein (FIG. 8 and ¶22), the opening defined by first and second cross-sectional dielectric sidewalls. A first conductive cross-sectional spacer (FIG. 10, element 100) is formed on the first dielectric sidewall wherein the first conductive spacer forms a portion of a capacitor top plate (¶12, line 7, and ¶34). A first capacitor cell dielectric layer (¶26, line 2, and FIG. 10, element 102) is formed on the first conductive spacer, and a second conductive cross-sectional spacer (FIG. 11, element 104, and ¶27) is formed on the first capacitor cell dielectric layer. A first conductive layer is (FIG. 13, element 130 and ¶29) formed on the second conductive spacer, wherein the second conductive spacer 104 and the first conductive layer 130 each form a portion of a capacitor bottom plate (¶38, lines 4 and 5). A second cell dielectric layer is formed on the first conductive layer (FIG. 15, element 150, and ¶32), a second conductive layer (FIG. 15, element 152 and ¶32, line 2) is formed on the second cell dielectric layer wherein the second conductive layer forms a portion of the capacitor top plate (¶37, line 5), and a conductive feature (FIG. 17, element 170 or FIG. 21, element 210) is formed which electrically connects the first conductive spacer 100 and the second conductive layer 152.

Dependent claim 2 recites prior to etching the base dielectric layer 32, forming a third conductive layer (FIG. 8, element 82 and ¶22) over a planarized surface of the base dielectric layer 32. Also, during the etching of the base dielectric layer to form the opening, etching the third conductive layer (depicted as etched layer 82 in FIG. 8) to form an opening in the third conductive layer and forming the

first conductive cross-sectional spacer (FIG. 10, element 100) to contact the third conductive layer 82. An etch is performed which forms a cross-sectional third sidewall (depicted as element 154 of FIG. 18, unnumbered in FIG. 20, ¶34) from the second conductive layer 152, the second cell dielectric layer 150, and the third conductive layer 82 (¶¶32-20). During the formation of the conductive feature, a conformal fourth conductive layer (FIG. 17, element 200, and ¶37) which contacts the second conductive layer 152 and the third conductive layer 82 is formed. The fourth conductive layer is spacer etched, which forms a third conductive cross-sectional spacer (element 210, FIG. 21) on the third sidewall and electrically connects the first conductive spacer 100 and the second conductive layer 152 through the third conductive layer 82.

Claim 3, which depends from claim 2, recites the formation of fourth and fifth conductive cross-sectional spacers (FIG. 21, element 212, and ¶37, last sentence) from the fourth conductive layer (FIG. 21, element 200) within the opening in the base dielectric layer during the spacer etch of the fourth conductive layer.

Claim 4 (and analogous claim 7) which depends from claim 2 (claim 6), recites removing at least a portion of the third conductive layer 82 using a planarizing process prior to forming the second cell dielectric layer 150 (performed on the FIG. 13 structure to result in the FIG. 14 structure, described in ¶31).

Claim 5 (and analogous claim 8) recites the method of claim 4 (of claim 7) further comprising removing a portion of each of the first conductive cross-sectional spacer 100, the first capacitor cell dielectric layer 102, the second conductive cross-sectional spacer 104, and the first conductive layer 130 during the planarizing process (¶31).

Claim 6, which depends from claim 1, recites prior to etching the base dielectric layer 32, forming a third conductive layer (FIG. 8, element 82 and ¶22) over a planarized surface of the base dielectric layer 32, and during the etching of the base dielectric layer to form the opening, etching the third conductive layer to form an opening in the third conductive layer (depicted as etched layer 82 in FIG. 8). Also, forming the first conductive cross-sectional spacer (FIG. 10, element

100) to contact the third conductive layer 82, etching the second conductive layer 152 (FIG. 16) and the second cell dielectric layer 150 to form an opening 162 therein (¶33) and to expose the third conductive layer 82, and forming a conductive plug (180, FIG. 18) within the opening 162 in the second conductive layer 152 and the second cell dielectric layer 150, the plug 162 contacting the second conductive layer 152 and the third conductive layer 82 to electrically connect the first conductive spacer 100 and the second conductive layer 152 through the third conductive layer 82 (¶34 and FIG. 18).

Independent claim 9 recites a method used to form a semiconductor device comprising providing a semiconductor wafer substrate assembly (FIG. 8, element 10, and ¶22) comprising a semiconductor wafer 12 and a conductive contact pad 28 overlying the wafer 12, forming an etch stop layer 80 on the contact pad 28, forming a blanket planarized base dielectric layer 32 on the etch stop layer 80, and forming a conformal first conductive layer 82 on the planarized base dielectric layer 32 (¶¶ 22, 23). The conformal first conductive layer 82 and the planarized base dielectric layers 32 are etched (¶24) to expose the etch stop 80 and to form first and second cross sectional sidewalls in the base dielectric layer 32. The sidewalls define a recess in the base dielectric layer 32. A second conductive layer 100 (FIG. 10) comprising a first conductive spacer on the first sidewall is formed, and a first cell dielectric layer 102 is formed on the first conductive spacer 100 and on the etch stop layer 80 (¶26). A third conductive layer 104 is formed on the first cell dielectric layer 102, and the third conductive layer and the first cell dielectric layer are spacer etched (between FIGS. 10 and 11, ¶27) to form a second conductive spacer (depicted as 104 in FIG. 11) from the third conductive layer 104, to form a cell dielectric spacer (102, FIG. 11) from the first cell dielectric layer 102, and to expose the etch stop 80 layer (¶27). After spacer etching the third conductive layer 104 and the first cell dielectric layer 102, the etch stop layer 80 is etched (as depicted in FIG. 12, ¶28) to expose the contact pad 28. A fourth conductive layer (130, FIG. 13) is formed on the second conductive spacer 104 and on the contact pad 28 (¶30), and a second cell dielectric layer 150 is formed on the fourth conductive layer 130 (¶32, and FIG. 15) A fifth conductive layer (152, FIG. 15 and ¶32) is formed on the second cell dielectric layer 150, and the first conductive spacer 100 and fifth conductive layer 152 are electrically connected (with plug 180

of FIG. 18 and ¶34, or spacer 210 of FIG. 21 and ¶37), wherein the second 100 and fifth 152 conductive layers form a first capacitor plate (¶34), and the third 104 and fourth 130 conductive layers form a second capacitor plate (¶38) interposed between the first conductive spacer 100 and the fifth conductive layer 152 (¶15).

Claim 10, depending from claim 9, recites that during the formation of the second conductive layer (90, FIG. 9), the spacer (100, FIG. 10, i.e. the first conductive spacer 100 comprised by the second conductive layer 90) is formed to contact the first conductive layer 82 (FIG. 10). An opening 162, FIG. 16 is etched in the second cell dielectric layer 150 and the fifth conductive layer 152 to expose the first conductive layer 82 (¶33), and a conductive plug 180 is formed within the opening 162 in the fifth conductive layer 152 and the second cell dielectric layer 150. The plug 162 contacts the first conductive layer 82 and the fifth conductive layer 152 to electrically connect the first conductive spacer 100 and the fifth conductive layer 152 through the first conductive layer 82 (¶34 and FIG. 18).

Claim 11 recites the method of claim 9, further comprising performing an etch which forms a third cross-sectional sidewall (depicted as element 154 of FIG. 18, unnumbered in FIG. 20, ¶34) from the fifth conductive layer 152, the second cell dielectric layer 150, and the first conductive layer 82 (FIG. 17). A sixth conductive layer (200, FIG. 20) is formed over the fifth conductive layer 152 and on the third cross-sectional sidewall 154, and the sixth conductive layer 200 is spacer etched to from a conductive spacer 210 on the third cross-sectional sidewall 154 which electrically connects the first conductive spacer 100 and the fifth conductive layer 152 (¶37, through layer 82).

Claim 12 recites the method of claim 11 further comprising, during the formation of the sixth conductive layer 200, forming a portion of the sixth conductive layer 200 within the opening in the base dielectric layer 32, wherein subsequent to spacer etching the sixth conductive layer 200, a portion 212 of the sixth conductive layer 200 remains in the opening in the base dielectric layer (¶37).

Independent claim 20 recites a method used to form a semiconductor device, comprising forming a semiconductor wafer substrate assembly (FIG. 8, element 10, and ¶22) comprising a base supporting layer 32, 82 having a recess therein (¶4). The method further comprises forming first 100 and second 104 conductive spacers having a first cell dielectric 102 interposed therebetween (FIG. 14 and ¶12) which electrically isolates the first and second conductive spacers from each other. A first conductive layer 130 electrically connected to the second conductive spacer 104 within the recess is formed, as is a blanket second conductive layer (152, FIG. 15) over the first conductive layer 130 and electrically separated from the first conductive layer by a second cell dielectric layer 150. The first conductive spacer 100 and the blanket second conductive layer 152 are electrically connected (with plug 180 and layer 82 of FIG. 18, or with spacer 210 and layer 82 of FIG. 21) to form a storage capacitor, where the first conductive spacer 100 and blanket second conductive layer 152 form a portion of a capacitor top plate (¶34), and the second conductive spacer 104 and first conductive layer 130 form a portion of a capacitor bottom plate (¶38).

Claim 21 depends from claim 20 and further comprises etching the blanket second conductive layer 130 prior to electrically connecting the first conductive spacer 100 and the blanket second conductive layer 152 (layer 130 may etched using chemical mechanical planarization on the FIG. 13 structure to result in the FIG. 14 structure, see ¶31).

Claim 22 depends from claim 21 and further comprises, during the formation of the base supporting layer, forming a base dielectric layer 32 and a base conductive layer 82 over the base dielectric layer 32, and etching the base conductive layer 82 and the base dielectric layer 32 to form the recess in the base supporting layer. Further, subsequent to the etching of the blanket second conductive layer 152, the base conductive layer 82 is etched to form a sidewall 154 defined by the blanket second conductive layer 152 and the base conductive layer 82 (¶34).

Claim 23 recites the method of claim 22 further comprising forming a third conductive spacer 210 over the sidewall 154 to electrically connect the blanket second conductive layer 152 and the base conductive layer 82 (¶37).

Claim 22, which depends from claim 22, recites etching the blanket second conductive layer 152 and the base conductive layer 82 to form an opening 162 therein, and forming a conductive plug 180 within the opening 162 to electrically connect the blanket second conducive layer 152 and the base conductive layer 82 (¶¶33, 34).

Independent claim 25 recites a method used to form a semiconductor device comprising a storage capacitor having a top plate and a bottom plate, comprising forming a first portion of a capacitor top plate comprising a vertically-oriented conductive spacer 100 (¶12, line 7, and ¶34), and forming a first cell dielectric layer 102 (¶26, line 2, and FIG. 10) to contact the first portion 100 of the capacitor top plate. The method further forms a first portion 104 of a capacitor bottom plate (¶38, lines 4 and 5) comprising a vertically-oriented conductive spacer to contact the first cell dielectric layer 102, and forming a second portion 130 of the capacitor bottom plate comprising a vertically-oriented layer to contact the first portion 104 of the capacitor bottom plate. A second cell dielectric layer 150 is formed to contact the second portion 130 of the capacitor bottom plate (FIG. 15). A second portion 152 of the capacitor top plate is formed to contact the second cell dielectric layer and which comprises a portion which overlies the first portion 100 of the capacitor top plate, the first 102 and second 150 cell dielectric layers, and the first 104 and second 130 portions of the capacitor bottom plate. Finally, a conductive structure (180, FIG. 18 or 210, FIG. 21) is formed which electrically connects the first 100 and second 152 capacitor top plate portions (through layer 82, FIGS. 18 and 21).

Claim 26 which depends from claim 25 recites that the formation of the conductive structure (FIG. 21, element 210) which electrically connects the first (FIG. 21, in this embodiment comprising layers 82, 100) and second 152 capacitor top plate portions comprises etching the first 82 and second 152 capacitor top plate portions to form a sidewall (154, FIG. 15) comprising the first 82, 100 and second 152 capacitor top plate portions, forming a blanket conductive layer (200, FIG. 20) on the sidewall, and etching the blanket conductive layer 200 to form a conductive spacer 210 which contacts the sidewall 154 and electrically connects the first 82, 100 and second 152 capacitor top plate portions (¶37).

Claim 27, which depends from claim 15 recites that the formation of the conductive structure which electrically connects the first 82, 100 and second 152 capacitor top plate portions comprises etching the first 82 and second 152 capacitor top plate portions to form an opening (162, FIG. 16) in the first 82 and second 152 capacitor top plate portions, and forming a conductive plug (FIG. 18, element 180) within the opening 162 in the first 82 and second 152 capacitor top plate portions.

Claim 28 recites the method of claim 25 further comprising providing a semiconductor wafer substrate assembly (10, FIG. 10) comprising a semiconductor wafer 12 having a conductively-doped region 14 therein and forming a conductive pad 28 to contact the conductively-doped region 14 of the semiconductor wafer 12. During the formation of the first portion 104 of the capacitor bottom plate, a blanket conductive bottom plate layer 104 (FIG. 10) is formed, then the conductive bottom plate layer 104 is spacer etched to form the first portion (104, FIG. 11) of the capacitor bottom plate having an opening therein (at FIG. 12) whereby the conductive pad 28 is exposed through the opening in a bottom of the bottom plate layer 104. It is further specified that the second portion 130 of the capacitor bottom plate layer is formed to contact the first portion 104 of the capacitor bottom plate layer and the conductive pad 28 through the opening in the first portion 104 of the bottom plate layer (as depicted in FIG. 13, ¶28).

VI. Ground Of Rejection To Be Reviewed On Appeal

Claims 1-12 and 20-28 stand rejected under 35 USC §102(e) over Zheng, et al. (US Pub. No. 2003/0166318).

VII. Argument

Rejection of all of pending claims 1-12 and 20-28 under 35 USC §102(e) over Zheng, et al. (Pub. US 2005/0026361 A1)

The Examiner has rejected claims 1-12 and 20-28 under 35 USC §102(e) over Zheng, et al. (US Patent Publication 2005/0026361 A1) in the final office action of September 30, 2005 (referred to hereinafter as "FOA") and has maintained the rejection in the advisory action of November 23, 2005 (referred to hereinafter as "AA").

It should be noted that the office actions, in most instances, do not specify the method acts and elements of Zheng which are being used to teach the method of the present invention. For example, see page 4 of the FOA, wherein present claim 2 is repeated, and the Examiner merely states that all the features are taught at paragraph [0012] FIGS. 1-2 of Zheng. No indication or explanation of what is being used to teach the claimed method is given. This is the dominant strategy for rejection throughout the office actions, and renders a rebuttal with any substance beyond "Zheng does not teach the recited method acts" difficult or impossible without extensive speculation on the part of the Applicants' agent. This must include speculation as to what method acts of Zheng are supposed to teach the method acts of the present claimed method with sufficient similarity to merit rejection under the standards required by 35 USC §102(e).

The dearth of precise points of rejection in the office actions was discussed in the "Request for Withdrawal of the Final Status of the September 30, 2005 Office Action as Being Premature and for Reconsideration of the Application," filed November 3, as well as the previous response to the initial office action. While a genuine attempt has been made to respond to the rejections of the claims, it is again submitted that, because the office actions largely omits any reference to specific method acts of Zheng being used as a basis of rejection, a meaningful response to assertions of the office actions is not possible without considerable speculation on the part of the Applicants' agent.

Description of the Art Relied Upon

All references in this section are to the text and drawings of Zheng. Zheng discloses a method for forming a double-sided capacitor for a semiconductor device comprising forming an opening 18 in a base dielectric layer 16 and forming a lower electrode layer 20, typically HSG polysilicon (line 9, ¶[0012]) which typically covers the entire inner surface of container 18 (lines 1 and 2, ¶[0013]). A dielectric 22 is formed on the lower electrode 20, then a reoxidized layer 24 is formed over the dielectric layer 22 by subjecting the dielectric layer 22 to a reoxidation process (lines 14, 15 of ¶[0012]). Finally, an upper electrode layer 26, typically polysilicon, is formed over the reoxidized layer 24. FIG. 3 depicts an additional oxide layer (unnumbered) formed over the top electrode 26 and within opening 18.

Thus with regard to FIGS. 2, Zheng recites the formation of two conductive layers (20, 26) and dielectric layers (22, 24) in opening 18. At FIG. 3, an additional dielectric layer (unnumbered) is formed within container 18 in dielectric layer 16. Conductive layer 20 is a lower (bottom) electrode, and conductive layer 26 is an upper (top) electrode. None of these layers forms a spacer. While Zheng does not detail the layout of the FIG. 3 cell (see ¶[0021], for example), with regard to FIG. 3 (reproduced and colored below), Zheng appears to recite the formation of only two sets of spacers: conventional dielectric spacers surrounding the transistor gates (unnumbered, depicted in yellow and hatched from lower left to upper right, which are also depicted in FIGS. 1 and 2), and spacers (unnumbered, depicted in red and hatched from upper left to lower right) which add height to the plates. Zheng does not appear to specify whether the unnumbered spacers in red are dielectric or conductive. Assuming *arguendo* that the spacers depicted in red are conductive, they must form part of the capacitor lower electrode (i.e. the bottom plate), at least because they physically contact layer 20 which Zheng calls the "lower electrode" (¶[0012], line 9).

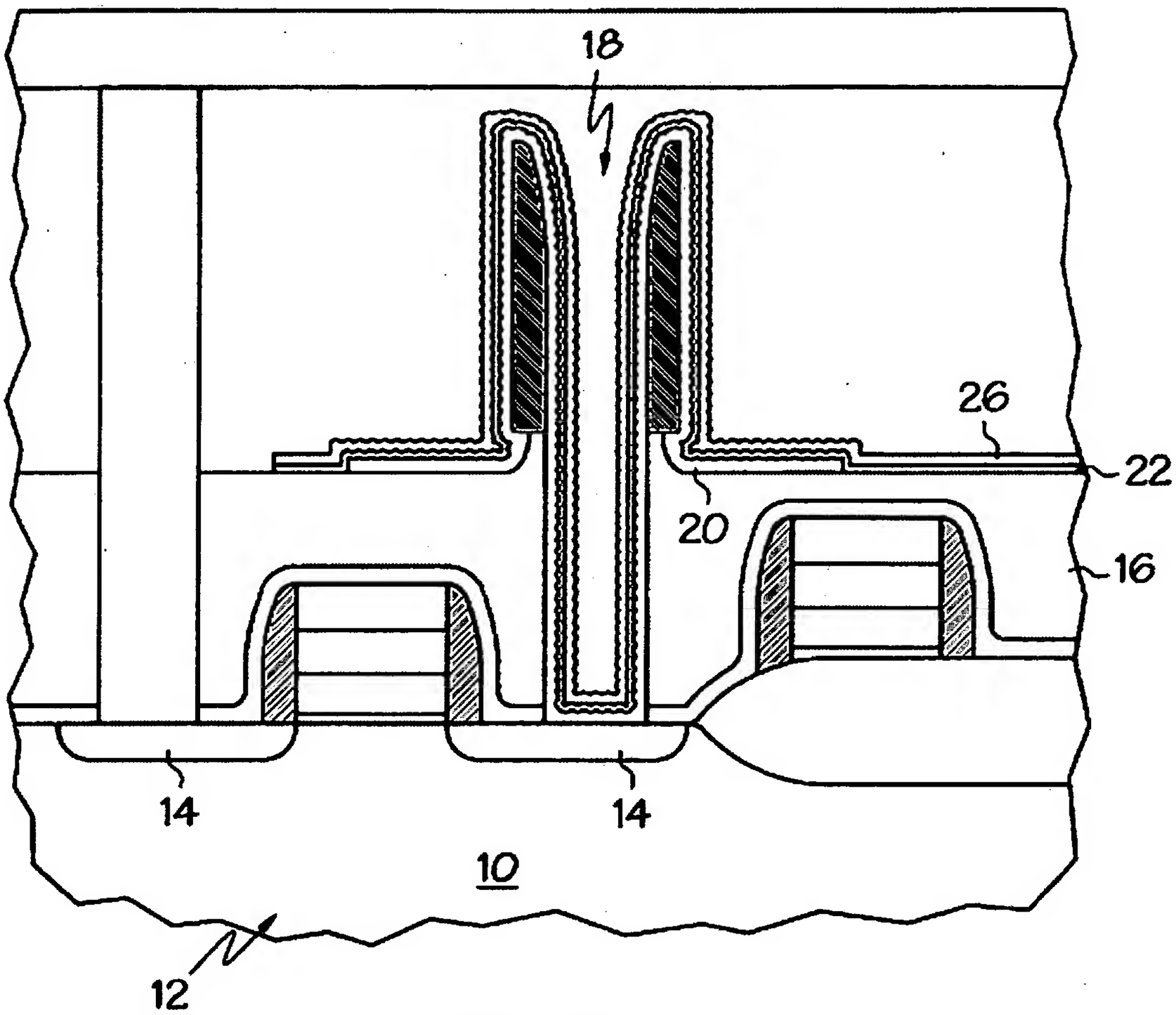


FIG. 3

Argument as to Patentability of Claim 1

The present invention as claimed recites patentable differences over the invention of Zheng. Claim 1 recites "forming a first conductive cross-sectional spacer on said first dielectric sidewall wherein said first conductive spacer forms a portion of a capacitor top plate; forming a first capacitor cell dielectric layer on said first conductive spacer; forming a second conductive cross sectional spacer on said first capacitor cell dielectric layer; forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate; forming a second cell dielectric layer on said first conductive layer...and forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer.

At ¶44 of the present application, it is specified that the term "on" is used with respect to two layers with at least some contact between the two layers (but does not imply directionality).

Zheng fails to describe "forming a first conductive cross sectional spacer wherein...said first conductive spacer forms a portion of a capacitor top plate." Zheng either does not describe a conductive spacer, or the unnumbered spacer depicted in red in FIG. 3 *supra* is part of the bottom plate as discussed above. Zheng also does not describe forming a first capacitor cell dielectric layer on the first conductive spacer and "forming a second conductive cross sectional spacer on said first capacitor cell dielectric layer." Zheng forms no conductive spacer on any cell dielectric layer. Zheng forms the upper electrode layer (i.e. the "top plate") to overlie the spacer in red, but the top plate is not formed as a spacer. As Zheng forms no second conductive spacer, it is not possible to form "a first conductive layer on said second conductive spacer."

Additionally, while the Examiner states that Zheng recites "a conductive feature (unlabeled) which electrically connects the first conductive spacer and the second conductive layer (FIG. 3)," (page 3, penultimate and ultimate lines) the Examiner has not indicated what FIG. 3 element is being formed to teach this recitation. No element can be discerned in FIG. 3 of Zheng by the Applicants' agent, the formation of which fulfills the recitation of claim 1 of "forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer." As it is not immediately obvious what method act taught by Zheng the Examiner is referring, the Applicants have not been given fair opportunity to reply. This was pointed out in the Applicants' response of July 19, 2005, and it is not evident that the additional, requested direction has been provided.

The Examiner uses layer 20 of Zheng to teach the formation of the "top plate" of the present invention (page 3, first paragraph). However, layer 20 of Zheng is the lower (bottom) electrode (¶[0012], line 9), and the formation of the lower electrode does not obviate the formation of the top plate under 35 USC §102(e). The Examiner uses the formation of some unspecified layer of Zheng as the bottom plate (page 3 lines 7-9), however the only capacitor cell layers in FIG. 2 which are conductive are layers 20 (the bottom electrode) and 26 (the top electrode). The Examiner uses both of layers 20 and 26 of FIG. 2 to teach the formation of the top electrode portions of the present invention, thus leaving the capacitor of FIG. 2 with no bottom plate.

Additionally, claim 1 recites "forming a first conductive layer on said second conductive spacer...". As indicated above, "on" indicates at least some contact between the two layers. If the only two conductive capacitor layers of FIG. 2 of Zheng (layers 20, the lower electrode, and 26, the top electrode) were formed to contact each other, the device would be nonfunctional.

The Examiner further asserts that FIG. 2 depicts "a first conductive cross sectional spacer on the first dielectric sidewall...[and] a second conductive cross-sectional spacer on the first capacitor cell dielectric layer." However, FIG. 2 depicts the formation of no conductive cross sectional spacers, and there is no conductive spacer formed on the first capacitor cell dielectric layer 22.

The Examiner states in the AA of November 23, 2005 "in response to Applicants' contention that Zheng does not appear to describe a first conductive cross-sectional spacer on the first dielectric sidewall and forming a second conductive cross-sectional spacer on the first capacitor cell dielectric layer...applicants are directed to FIG. 3, wherein Zheng discloses forming a first conductive cross-sectional spacer 20 on the first dielectric sidewall of insulating layer 16; forming a first capacitor cell dielectric layer 22 on the first conductive spacer; and forming a second conductive cross-sectional spacer 26 on the first capacitor cell dielectric layer 22 (page 1 paragraphs [0012]-[0014])."

It should be noted that layers 20 and 26 are not "spacers" as the term is conventionally used in the semiconductor industry. While FIG. 3 does depict spacers, they are specifically the unnumbered elements of FIG. 3 depicted *supra* in red and in yellow. Further, claim 1 specifies that the "first conductive cross-sectional spacer forms a portion of a capacitor top plate" and the "second conductive spacer...form[s] a portion of a capacitor bottom plate." The Examiner appears to indicate that the recitation of a capacitor bottom plate and top plate carries no weight, because "applicants do not show how the first conductive cross-sectional spacer form a portion of a capacitor top plate and that the second conductive spacer form a portion of a capacitor bottom plate." The depiction of the elements in the present application, for example at FIG. 18 and the text in the application (¶¶34 and 35, for example) provides sufficiently detailed information to enable one of ordinary skill in the art to determine how the recited elements form a capacitor bottom plate and a capacitor top plate.

Clearly, the use of the features of Zheng as applied by the Examiner to reject the present invention as claimed is not reasonable. The use of Zheng as applied by the Examiner is respectfully traversed, for example because it is not reasonable to use both the capacitor bottom and top plate of Zheng to teach the top plate of the present invention as claimed and, thus leave the storage capacitor of Zheng with no bottom plate. The Examiner has used Zheng as a source of a mere catalog of elements in an attempt to improperly formulate an anticipation rejection, without addressing the claimed relationships between those elements and, more significantly, the method acts as recited in claim 1, which cannot be supported due to the deficiencies in the structure described in Zheng.

The claim chart below summarizes some of the differences between claim 1 and the disclosure of Zheng.

Claim 1	Zheng	Office Action and Applicants' Comments
forming a first conductive cross-sectional *spacer* on said first dielectric sidewall wherein said first conductive spacer forms a portion of a *capacitor top plate*	does not appear to describe forming a conductive spacer. forms a *bottom electrode blanket layer* 20 (not spacer) on the sidewall (¶12, line 9)	uses bottom plate blanket layer 20 to teach the formation of recited top plate spacers
forming first capacitor cell dielectric layer on said first conductive spacer	forms dielectric 22 on blanket lower electrode	uses dielectric 22 formed on blanket lower plate to teach forming a dielectric on first conductive [upper plate] spacer
forming a second conductive cross-sectional spacer on said first capacitor cell dielectric layer	does not appear to describe second conductive spacer on first capacitor cell dielectric layer	Examiner states at page 3, lines 5, 6 that second conductive spacer on first capacitor cell dielectric is taught, does not indicate what is used to describe the formation of these layers
forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate	forms upper electrode layer 26 on reox layer 24, not on any conductive spacer	though Examiner does not indicate what layer is used to teach the formation of the "first conductive layer on said second conductive spacer" it appears that it must be layer 26. This is the capacitor upper electrode, not the bottom plate which is presently claimed (however, see also comments two rows below)
forming a second cell dielectric layer on said first conductive layer	forms dielectric 22 and reox 24 on dielectric 22	Examiner has used layer 22 to teach first cell dielectric layer. Layer 24 is formed prior to forming layer 26, therefore not formed on layer 26
forming a second conductive layer on said second cell dielectric layer, wherein said second conductive layer forms a portion of said capacitor top plate	forms top plate 26	Examiner uses layer 26 as top plate, but also appears to use layer 26 to teach "first conductive layer" which is part of "bottom plate" (see two rows above). Thus uses the formation of a single layer to describe the formation of both a capacitor bottom plate and a capacitor top plate
forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer	no conductive feature is formed to connect layer 20 (which Examiner uses as first conductive top plate spacer) to layer 26 (which Examiner uses as top plate).	Examiner uses "unlabeled" structure as describing this, does not indicate what this is. Only two conductive plate layers appear to be 20 (lower electrode) and 26 (upper electrode). If present, this would short bottom plate to top plate according to Examiner's teachings. If upper spacer pair of Zheng FIG. 3 is conductive, it contacts bottom plate 20 and is therefore part of bottom plate.

Argument as to Patentability of Claim 2

Regarding claim 2, the Examiner states that Zheng discloses "prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer, and forming said first conductive cross sectional spacer to contact said third conductive layer." However, the Examiner has not indicated what is used in FIGS. 1 and 2 of Zheng to depict forming the third conductive layer over a planarized surface of the base dielectric layer prior to etching the base dielectric layer and forming the first conductive cross sectional spacer to contact the third conductive layer. It does not appear that forming such a layer is described by Zheng at page 1 ¶[0012] and FIGS. 1-2 as stated by the Examiner.

Argument as to Patentability of Claim 3

Regarding claim 3, the Examiner submits that "Zheng discloses forming fourth and fifth conductive cross-sectional spacers from said fourth conductive layer within said opening in said base dielectric layer during said spacer etch of said fourth conductive layer (page 1, paragraph [0012] and FIGS. 1-2)." Zheng at best depicts two conductive cross-sectional spacers, specifically the red spacers at FIG. 3 as depicted *supra*, which themselves may be dielectric spacers. Zheng does not discuss forming fourth and fifth conductive cross-sectional spacers at the location indicated by the Examiner; thus, claim 3 is further allowable over the cited art as applied by the Examiner. It appears that only two conductive layers are formed within the opening 18 in dielectric layer 16, the lower electrode 20 and the upper electrode 26, neither of which are spacers.

Argument as to Patentability of Claim 4

Regarding claim 4, the Examiner states that at paragraph [0012] and FIGS. 1-2, Zheng discloses "removing at least a portion of said third conductive layer using a planarizing process prior to forming said second cell dielectric layer." Zheng does not appear to disclose forming a third conductive layer over a planarized surface of the base dielectric layer prior to etching the base dielectric layer 16 (which results in the formation of opening 18) as recited in claim 2 from which claim 4 depends, nor removing at least a portion of the third conductive layer using a planarizing process prior to forming the second cell dielectric layer. In the paragraph specified by the Examiner, only two conductive capacitor layers are described, layer 20 (the lower electrode) and layer 26 (the upper electrode), and there is no planarizing process described.

Argument as to Patentability of Claim 5

Regarding claim 5, the Examiner states that at page 1, paragraph [0012] and FIGS. 1-2, Zheng discloses "removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross sectional spacer, and said first conductive layer during said planarizing process." However, at the cited text and FIGS. 1-2, there is no planarizing process described. While it might be argued that lower electrode 20 *could* be formed using a planarizing process (see lower electrode 20 at FIG. 1), this is not discussed, and dielectric 22, reox layer 24, and upper electrode 26 are clearly formed *after* this planarization of layer 20. This is contrary to the claim 5 recitation of "removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process," which is clearly absent from the location the Examiner cites.

Argument as to Patentability of Claim 6

With regard to claim 6, the Examiner states that Zheng discloses at page 1, paragraph [0012] and FIGS. 1-2 "prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer; during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer; forming said first conductive cross-sectional spacer to contact said third conductive layer; etching said second conductive layer and said second cell dielectric layer to form an opening therein and to expose said third conductive layer; forming a conductive plug within said opening in said second conductive layer and said second cell dielectric layer, said plug contacting said second conductive layer and said third conductive layer to electrically connect said first conductive spacer and said second conductive layer through said third conductive layer." The Examiner does not indicate what features of Zheng are being used to correspond to the elements of claim 6; however, it appears that Zheng does not describe *any* of these claimed method acts. Zheng does not describe forming a third conductive layer over a planarized surface of the base dielectric layer (presumably layer 16) prior to etching and, therefore, cannot describe forming an opening in the third dielectric layer, forming the spacer to contact the third conductive layer, etc.

Argument as to Patentability of Claims 7 and 8

With regard to claims 7 and 8, as Zheng apparently fails to describe a third conductive layer (the Examiner has not indicated what is being used as the formation of the third conductive layer) and describes no planarizing act at the specified location, Zheng necessarily fails to describe the method of claims 7 and 8.

It appears that Zheng fails to describe at least the following processing acts found in claim 9: providing a contact pad, forming an etch stop layer on the contact pad, forming a blanket planarized base dielectric layer on the etch stop layer; etching the conformal first conductive layer and the planarized base dielectric layer to form first and second cross sectional sidewalls in the base dielectric layer which define a recess in the base dielectric layer, wherein the etch exposes the etch stop layer; forming a second conductive layer which comprises a first conductive spacer on the first sidewall; forming a first cell dielectric layer on the etch stop layer; forming a third conductive layer on the first cell dielectric layer; spacer etching the third conductive layer and the first cell dielectric layer to form a second conductive spacer from the third conductive layer, to form a cell dielectric spacer from the first cell dielectric layer, and to expose the etch stop layer; subsequent spacer etching the third conductive layer and the first cell dielectric layer, etching the etch stop layer to expose the contact pad; forming a fourth conductive layer on the second conductive spacer and on the contact pad; forming a second cell dielectric layer on the fourth conductive layer; forming a fifth conductive layer on the second cell dielectric layer; and electrically connecting the first conductive spacer and the fifth conductive layer, wherein the second and fifth conductive layers form a first capacitor plate and the third and fourth conductive layers form a second capacitor plate interposed between the first conductive spacer and the fifth conductive layer.

Argument as to Patentability of Claim 10

It appears that Zheng fails to describe at least the following processing acts found in claim 10: during said formation of said second conductive layer, forming said spacer [i.e. the first conductive spacer comprised by the second conductive layer] to contact said first conductive layer; etching an opening in said second cell dielectric layer and said fifth conductive layer to expose said first conductive layer; forming a conductive plug within said opening in said fifth conductive layer and said second cell dielectric layer, said plug contacting said first conductive layer and said fifth conductive layer to electrically connect said first conductive spacer and said fifth conductive layer through said first conductive layer.

Argument as to Patentability of Claim 11

It appears that Zheng fails to describe at least the following processing acts found in claim 11: performing an etch which forms a third cross-sectional sidewall from said fifth conductive layer, said second cell dielectric layer, and said first conductive layer; forming a sixth conductive layer over said fifth conductive layer and on said third cross-sectional sidewall; and spacer etching said sixth conductive layer to form a conductive spacer on said third cross-sectional sidewall which electrically connects said first conductive spacer and said fifth conductive layer.

Argument as to Patentability of Claim 12

It appears that Zheng fails to describe at least the following processing acts found in claim 12: during said formation of said sixth conductive layer, forming a portion of said sixth conductive layer within said opening in said base dielectric layer, wherein subsequent to spacer etching said sixth conductive layer, a portion of said sixth conductive layer remains in said opening in said base dielectric layer.

Argument as to Patentability of Claim 20

It appears that Zheng fails to describe at least the following processing acts found in claim 20: within a recess in a base supporting layer, forming first and second conductive spacers having a first cell dielectric layer interposed therebetween which electrically isolates the first and second conductive spacers

from each other; forming a first conductive layer electrically connected to the second conductive spacer within the recess; forming a first conductive layer electrically connected to the second conductive spacer within the recess; and electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where the first conductive spacer and blanket second conductive layer form a portion of a capacitor top plate and the second conductive spacer and first conductive layer form a portion of a capacitor bottom plate.

The claim chart below summarizes some of the differences between the processing acts claim 20 and the disclosure of Zheng.

Claim 20	Zheng	Office Action and Applicants' Comments
within the recess in the base supporting layer, forming first and second conductive spacers having a first cell dielectric interposed therebetween which electrically isolates the first and second conductive spacers from each other	describes forming a bottom electrode 20 within the recess 18 and a top electrode 26 within recess 18. cell dielectric 22 electrically isolates bottom electrode from top electrode	Examiner uses layer 20 by itself as the first and second conductive spacers having a first cell dielectric interposed therebetween which isolates the first and second conductive spacers from each other. Layer 20, however, is a single connected layer, therefore electrically shorted, and not electrically isolated from each other by layer 22
forming a first conductive layer electrically connected to the second conductive spacer within the recess	Zheng forms no first conductive layer electrically connected to the second conductive spacer (layer 20, by Examiner's teaching) within recess 18	at page 9 lines 6-8 states that Zheng teaches forming a first conductive layer electrically connected to the second conductive spacer within the recess (p.1 ¶12 and FIG. 1), however FIG. 1 shows does not appear to show conductive layer connected to layer 20. 14 forms part of the recess, and is not in the recess
forming a blanket second conductive layer over the first conductive layer and electrically separated from the first conductive layer by a second cell dielectric layer	Zheng forms dielectrics 22 and 24, then forms top electrode 26. dielectrics 22 and 24 separate bottom electrode 20 from top electrode 26	Examiner states this is taught. the only blanket conductive layer formed over layer 20 is layer 26, the top electrode

electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where first conductive spacer and the blanket second conductive layer form a portion of a capacitor top plate and the second conductive spacer and the first conductive layer form a portion of a capacitor bottom plate	Zheng describes only conductive layer 20 (bottom electrode) and conductive layer 26 (top electrode)	Examiner states Zheng teaches electrically connecting the first conductive spacer (he uses layer 20 to teach this) and the blanket second conductive layer (he uses layer 26 to teach this). This would short Zheng's top and bottom electrodes together. Further, the Examiner uses layer 20 to teach both the first and second conductive spacers, which as claimed form part of the top plate and the bottom plate respectively. However, layer 20 is a single layer and cannot form both part of the top plate and the bottom plate.

Argument as to Patentability of Claim 21

It appears that Zheng fails to describe at least the following processing acts found in claim 21: etching the blanket second conductive layer prior to electrically connecting the first conductive spacer and the blanket second conductive layer.

Argument as to Patentability of Claim 22

It appears that Zheng fails to describe at least the following processing acts found in claim 22: during the formation of the base supporting layer, forming a base dielectric layer and a base conductive layer over the base dielectric layer; etching the base conductive layer and the base dielectric layer to form the recess in the base supporting layer; and subsequent to the etching of the blanket second conductive layer, etching the base conductive layer to form a sidewall defined by the blanket second conductive layer and the base conductive layer.

Argument as to Patentability of Claim 23

It appears that Zheng fails to describe at least the following processing acts found in claim 23: forming a third conductive spacer over the sidewall to electrically connect the blanket second conductive layer and the base conductive layer.

Argument as to Patentability of Claim 24

It appears that Zheng fails to describe at least the following processing elements found in claim 24: etching the blanket second conductive layer and the base conductive layer to form an opening therein; and forming a conductive plug within the opening to electrically connect the blanket second conductive layer and the base conductive layer.

Argument as to Patentability of Claim 25

With regard to claim 25, it appears that Zheng fails to describe at least the following processing acts: forming a first cell dielectric layer to contact the first portion of the capacitor top plate; forming a first portion of a capacitor bottom plate comprising a vertically-oriented conductive spacer to contact the first cell dielectric layer; forming a second portion of the capacitor bottom plate comprising a vertically oriented layer to contact the first portion of the capacitor bottom plate; forming a second cell dielectric layer to contact the second portion of the capacitor bottom plate; forming a second portion of the capacitor top plate to contact the second cell dielectric layer and which comprises a portion which overlies the first portion of the capacitor top plate, the first and second cell dielectric layers, and the first and second portions of the capacitor bottom plate; and forming a conductive structure which electrically connects the first and second capacitor top plate portions.

Argument as to Patentability of Claim 26

It appears that Zheng fails to describe at least the following processing acts found in claim 26: etching the first and second capacitor top plate portions to form a sidewall comprising the first and second capacitor top plate portions; forming a blanket conductive layer on the sidewall; and etching the blanket conductive layer to form a conductive spacer which contacts the sidewall and electrically connects the first and second capacitor top plate portions.

Argument as to Patentability of Claim 27

It appears that Zheng fails to describe at least the following processing acts found in claim 27: etching the first and second capacitor top plate portions to form an opening in the first and second capacitor top plate portions; and forming a conductive plug within the opening in the first and second capacitor top plate portions.

Argument as to Patentability of Claim 28

It appears that Zheng fails to describe at least the following processing acts found in claim 28: forming a conductive pad to contact the conductively-doped region of the semiconductor wafer; during the formation of the first portion of the capacitor bottom plate, forming a blanket conductive bottom plate layer and spacer etching the blanket conductive bottom plate layer to form the first portion of the capacitor bottom plate having an opening therein whereby the conductive pad is exposed through the opening in a bottom of the bottom plate layer; and forming the second portion of the capacitor bottom plate to contact the first portion of the capacitor bottom plate layer and the conductive pad through the opening in the first portion of the bottom plate layer.

It is therefore submitted the above-stated deficiencies in the disclosure of Zheng with respect to Applicants' claimed invention clearly demonstrate that claims 1-12 and 20-28 are patentable over Zheng, et al. under 35 USC §102(e). The Examiner's rejections of claims 1-12 and 20-28 over Zheng, et al. are respectfully traversed.

VIII. Claims Appendix

A copy of claims 1 through 12 and 20 through 28 is appended hereto as a CLAIMS APPENDIX.

IX. Evidence Appendix

No evidence pursuant to 37 CFR §§1.130, 1.131, or 1.132 was submitted during prosecution of the above-referenced patent application. Therefore, no such evidence has been relied upon by Appellants in this Appeal.

As required by 37 CFR §41.37(c)(1)(ix), the only "other evidence entered by the examiner and relied upon by appellant in the appeal" includes Zheng, et al. (US Pub. No. 2003/0166318), of record. Since a copy of this reference is present in the record, no EVIDENCE APPENDIX is required and an additional copy of this document is not provided with this Appeal Brief.

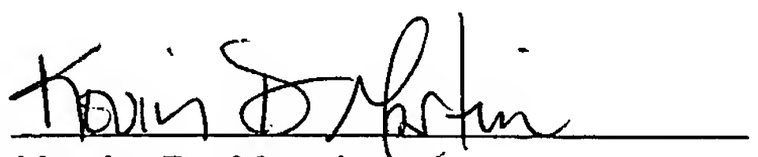
X. Related Proceedings Appendix

No decision(s) have been rendered by a court or by the Board in any proceeding identified in Section 2 of the Appeal Brief. Therefore, no RELATED PROCEEDINGS APPENDIX is required.

B. Conclusion

For the foregoing reasons, the applicants submit that claims 1-12 and 20-28 are clearly not anticipated by the disclosure of the cited reference and, therefore, are allowable. Accordingly, applicants respectfully request the reversal of the Examiner's rejection of claims 1-12 and 20-28.

Respectfully submitted,



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Claims Appendix

1. A method for forming a semiconductor device capacitor, comprising:

providing a base dielectric layer;

etching said base dielectric layer to form an opening therein, said opening defined by first and second cross-sectional dielectric sidewalls;

forming a first conductive cross-sectional spacer on said first dielectric sidewall wherein said first conductive spacer forms a portion of a capacitor top plate;

forming a first capacitor cell dielectric layer on said first conductive spacer;

forming a second conductive cross-sectional spacer on said first capacitor cell dielectric layer;

forming a first conductive layer on said second conductive spacer, wherein said second conductive spacer and said conductive layer each form a portion of a capacitor bottom plate;

forming a second cell dielectric layer on said first conductive layer;

forming a second conductive layer on said second cell dielectric layer, wherein said second conductive layer forms a portion of said capacitor top plate; and

forming a conductive feature which electrically connects said first conductive spacer and said second conductive layer.

2. The method of claim 1, further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

performing an etch which forms a cross-sectional third sidewall from said second conductive layer, said second cell dielectric layer, and said third conductive layer; and

during said formation of said conductive feature:

forming a conformal fourth conductive layer which contacts said second conductive layer and said third conductive layer;

spacer etching said forth conductive layer which forms a third conductive cross-sectional spacer on said third sidewall and electrically connects said first conductive spacer and said second conductive layer through said third conductive layer.

3. The method of claim 2 further comprising forming fourth and fifth conductive cross-sectional spacers from said fourth conductive layer within said opening in said base dielectric layer during said spacer etch of said fourth conductive layer.

4. The method of claim 2 further comprising removing at least a portion of said third conductive layer using a planarizing process prior to forming said second cell dielectric layer.

5. The method of claim 4 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

6. The method of claim 1 further comprising:

prior to etching said base dielectric layer, forming a third conductive layer over a planarized surface of said base dielectric layer;

during said etching of said base dielectric layer to form said opening, etching said third conductive layer to form an opening in said third conductive layer;

forming said first conductive cross-sectional spacer to contact said third conductive layer;

etching said second conductive layer and said second cell dielectric layer to form an opening therein and to expose said third conductive layer;

forming a conductive plug within said opening in said second conductive layer and said second cell dielectric layer, said plug contacting said second conductive layer and said third conductive layer to electrically connect said first conductive spacer and said second conductive layer through said third conductive layer.

7. The method of claim 6 further comprising removing at least a portion of said third conductive layer by a planarizing process prior to forming said second cell dielectric layer.

8. The method of claim 7 further comprising removing a portion of each of said first conductive cross-sectional spacer, said first capacitor cell dielectric layer, said second conductive cross-sectional spacer, and said first conductive layer during said planarizing process.

9. A method used to form a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer and a conductive contact pad overlying said wafer;

forming an etch stop layer on said contact pad;

forming a blanket planarized base dielectric layer on said etch stop layer;

forming a conformal first conductive layer on said planarized base dielectric layer;

etching said conformal first conductive layer and said planarized base dielectric layer to form first and second cross sectional sidewalls in said base dielectric layer which define a recess in said base dielectric layer, wherein said etch exposes said etch stop layer;

forming a second conductive layer which comprises a first conductive spacer on said first sidewall;

forming a first cell dielectric layer on said first conductive spacer and on said etch stop layer;

forming a third conductive layer on said first cell dielectric layer;

spacer etching said third conductive layer and said first cell dielectric layer to form a second conductive spacer from said third conductive layer, to form a cell dielectric spacer from said first cell dielectric layer, and to expose said etch stop layer;

subsequent to said spacer etching said third conductive layer and said first cell dielectric layer, etching said etch stop layer to expose said contact pad;

forming a fourth conductive layer on said second conductive spacer and on said contact pad;

forming a second cell dielectric layer on said fourth conductive layer;

forming a fifth conductive layer on said second cell dielectric layer; and

electrically connecting said first conductive spacer and said fifth conductive layer, wherein said second and fifth conductive layers form a first capacitor plate, and said third and fourth conductive layers form a second capacitor plate interposed between said first conductive spacer and said fifth conductive layer.

10. The method of claim 9 further comprising:

during said formation of said second conductive layer, forming said spacer to contact said first conductive layer;

etching an opening in said second cell dielectric layer and said fifth conductive layer to expose said first conductive layer;

forming a conductive plug within said opening in said fifth conductive layer and said second cell dielectric layer, said plug contacting said first conductive layer and said fifth conductive layer to electrically connect said first conductive spacer and said fifth conductive layer through said first conductive layer.

11. The method of claim 9 further comprising:

performing an etch which forms a third cross-sectional sidewall from said fifth conductive layer, said second cell dielectric layer, and said first conductive layer;

forming a sixth conductive layer over said fifth conductive layer and on said third cross-sectional sidewall; and

spacer etching said sixth conductive layer to form a conductive spacer on said third cross-sectional sidewall which electrically connects said first conductive spacer and said fifth conductive layer.

12. The method of claim 11 further comprising, during said formation of said sixth conductive layer, forming a portion of said sixth conductive layer within said opening in said base dielectric layer, wherein subsequent to spacer etching said sixth conductive layer, a portion of said sixth conductive layer remains in said opening in said base dielectric layer.

20. A method used to form a semiconductor device, comprising:

forming a semiconductor wafer substrate assembly comprising a base supporting layer having a recess therein;

within the recess in the base supporting layer, forming first and second conductive spacers having a first cell dielectric interposed therebetween which electrically isolates the first and second conductive spacers from each other;

forming a first conductive layer electrically connected to the second conductive spacer within the recess;

forming a blanket second conductive layer over the first conductive layer and electrically separated from the first conductive layer by a second cell dielectric layer; and

electrically connecting the first conductive spacer and the blanket second conductive layer to form a storage capacitor, where the first conductive spacer and blanket second conductive layer form a portion of a capacitor top plate and the second conductive spacer and first conductive layer form a portion of a capacitor bottom plate.

21. The method of claim 20 further comprising etching the blanket second conductive layer prior to electrically connecting the first conductive spacer and the blanket second conductive layer.

22. The method of claim 21 further comprising:

during the formation of the base supporting layer:

forming a base dielectric layer and a base conductive layer over the base dielectric layer;

etching the base conductive layer and the base dielectric layer to form the recess in the base supporting layer; and

subsequent to the etching of the blanket second conductive layer, etching the base conductive layer to form a sidewall defined by the blanket second conductive layer and the base conductive layer.

23. The method of claim 22 further comprising forming a third conductive spacer over the sidewall to electrically connect the blanket second conductive layer and the base conductive layer.

24. The method of claim 22 further comprising:

etching the blanket second conductive layer and the base conductive layer to form an opening therein; and

forming a conductive plug within the opening to electrically connect the blanket second conductive layer and the base conductive layer.

25. A method used to form a semiconductor device comprising a storage capacitor having a top plate and a bottom plate, comprising:

forming a first portion of a capacitor top plate comprising a vertically-oriented conductive spacer;

forming a first cell dielectric layer to contact the first portion of the capacitor top plate;

forming a first portion of a capacitor bottom plate comprising a vertically-oriented conductive spacer to contact the first cell dielectric layer;

forming a second portion of the capacitor bottom plate comprising a vertically-oriented layer to contact the first portion of the capacitor bottom plate;

forming a second cell dielectric layer to contact the second portion of the capacitor bottom plate;

forming a second portion of the capacitor top plate to contact the second cell dielectric layer and which comprises a portion which overlies the first portion of the capacitor top plate, the first and second cell dielectric layers, and the first and second portions of the capacitor bottom plate; and

forming a conductive structure which electrically connects the first and second capacitor top plate portions.

26. The method of claim 25 wherein the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises:

etching the first and second capacitor top plate portions to form a sidewall comprising the first and second capacitor top plate portions;

forming a blanket conductive layer on the sidewall;

etching the blanket conductive layer to form a conductive spacer which contacts the sidewall and electrically connects the first and second capacitor top plate portions.

27. The method of claim 25 wherein the formation of the conductive structure which electrically connects the first and second capacitor top plate portions comprises:

etching the first and second capacitor top plate portions to form an opening in the first and second capacitor top plate portions; and

forming a conductive plug within the opening in the first and second capacitor top plate portions.

28. The method of claim 25 further comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer having a conductively-doped region therein;

forming a conductive pad to contact the conductively-doped region of the semiconductor wafer;

during the formation of the first portion of the capacitor bottom plate:

forming a blanket conductive bottom plate layer; and

spacer etching the blanket conductive bottom plate layer to form the first portion of the capacitor bottom plate having an opening therein whereby the conductive pad is exposed through the opening in a bottom of the bottom plate layer; and

forming the second portion of the capacitor bottom plate to contact the first portion of the capacitor bottom plate layer and the conductive pad through the opening in the first portion of the bottom plate layer.

Evidence Appendix

None Submitted

Related Proceedings Appendix

None Cited

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PTO/SB/17 (01-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500

Complete if Known	
Application Number	10/628,994
Filing Date	July 28, 2003
First Named Inventor	Thomas M. Graettinger et al.
Examiner Name	Khiem D. Nguyen
Art Unit	2823
Attorney Docket No.	2003-0236.00/US

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 13-3092 Deposit Account Name: Micron Technology, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
21	- 20 or HP =		x		=	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
4	- 3 or HP =		x		=	

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
	- 100 =		/ 50 =		(round up to a whole number) x		=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Brief in Support of Appeal	$500

SUBMITTED BY

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Name (Print/Type)	Kevin D. Martin		Date February 22, 2006